PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference ASPE 3 PCT	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/FI2005/000104	International filing date *(day/month/year)* 17.02.2005	Priority date *(day/month/year)* 17.02.2004
International Patent Classification (IPC) or national classification and IPC INV. G02B6/43		
Applicant ASPOCOMP TECHNOLOGY OY et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 3 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
16.12.2005	16.05.2006
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Jones, J Telephone No. +49 89 2399-5887

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/FI2005/000104

Box No. I Basis of the report

1. With regard to the **language**, this report is based on

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3(a) and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4(a))
   - ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-14	as originally filed
Claims, Numbers	
1-16	received on 28.04.2006 with letter of 28.04.2006
Drawings, Sheets	
1/5-5/5	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/FI2005/000104

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-16
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-11
	No:	Claims	12-16
Industrial applicability (IA)	Yes:	Claims	1-16
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement.

Reference is made to the following documents:
D1: EP-A2-1 376 180
D2: US6684007 B2 YOSHIMURA TETSUZO ET AL 27 MARCH 2004 (2004-01-27).

1. Novelty.

Document D1 is regarded as being the closest prior art to the subject-matter of Independent claim 1, and shows (the references in parentheses applying to this document):

A method for embedding a component at least partly inside a circuit board, which component comprises an optically active area (abstract) and which circuit board comprises alternating conductor layers and insulating layers (claim 4, line 60-line 61), as well as at least one optical bus (claim 4, line 55), characterized in that a recess is formed at the component's embedding location, in such a way that the recess intersects the optical bus (claim 4, page 47 line 64-line 48, line 3)

The subject-matter of Independent claim 1 differs from that of D1 in that:

The component, which includes on one side both the optically active area, which is a surface that can transmit and/or receive light, and at least one conductive area, is set in place in such a way that the optically active area of the component comes into the vicinity of the intersection surface of the optical bus and the surface of the optically active area is at essentially right angles to the surface of the circuit board and the area or areas of conductive material are connected electrically to the conductor layer located on the surface of the circuit board, which is on the side of the embedding of the component.

The subject-matter of independent claim 1 is therefore new (Article 33(2) PCT).

The problem to be solved by the present invention may be regarded as to provide a method of embedding an optical component in a circuit board and in which the optical coupling loss to or from the optical component is low.

The solution to this problem proposed in independent claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) because in the current application the method of embedding the optical component does not require the use of clean room equipment and special semiconductor equipment, thus reducing manufacturing costs. Furthermore light is directly coupled to and from the device, thus avoiding optical losses when compared with those associated with commonly employed 45 degree mirrors.

Claims 2-11.
Claims 2-11 are dependent on claim 1 and as such also appear to meet the requirements of the PCT with respect to novelty and inventive step.

Claims 12-16.
Independent claim 12 and dependent claims 13-16 exactly correspond to original claims 13-17 are thus open to the same objections to inventive step as given in the communication of 29 March 2006.

The subject matter of the claims 1-16 complies with Article 33(4) PCT with respect to industrial applicability.

Claims:

1. A method for embedding a component (8) at least partly inside a circuit board, which component comprises an optically active area (11) and which circuit board comprises alternating conductor layers (1) and insulating layers (2), as well as at least one optical bus (3), characterized in that

- a recess (4) is formed at the component's (8) embedding location, in such a way that the recess intersects the optical bus (3),
- the component, which includes on one side both the optically active area (11), which is a surface that can transmit and/or receive light, and at least one conductive area (10, 12), is set in place in such a way that the optically active area (11) of the component comes into the vicinity of the intersection surface of the optical bus and the surface of the optically active area is at essentially right angles to the surface of the circuit board and the area or areas (10, 12) of conductive material are connected electrically to the conductor layer (1) located on the surface of the circuit board, which is on the side of the embedding of the component.

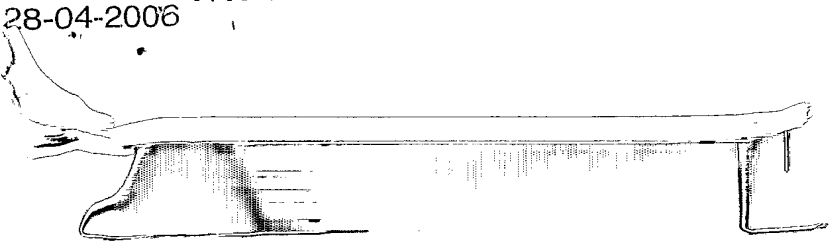
2. A method according to claim 1, characterized in that, when forming the recess (4), only material or materials, which do not act as an electrical transfer path (1), are removed from the circuit board.

3. A method according to claim 1 or 2, characterized in that transparent insulating material (9) is brought to the recess (4) remaining around the component after embedding, in such a way that the insulating material fill the space between the optically active area and the intersection surface of the optical bus.

4. A method according to claim 3, characterized in that the recess (4) remaining around the component after embedding is entirely filled with insulating material (9).

5. A method according to claim 3 or 4, characterized in that a pit is left or formed in the upper part of the recess (4), and is filled with a conductive material (13).

6. A method according to claim 5, characterized in that the electrically conductive material (13), with which the recess is filled, is a conductive polymer, a conductive adhesive, or



7. A method according to any of the above claims, characterized in that the side of the component facing the optical bus includes an optically active area (11) and an area or areas (10, 12) of a conductive material.

8. A method according to any of the above claims, characterized in that the side of the component facing away from the optical bus, or an adjacent side comprises an area (10) of a conductive material.

9. A method according to claim 8, characterized in that the component's area (10) of conductive material is connected electrically to the conductor layer (1) located on the surface of the circuit board beneath the component embedding location.

10. A method according to any of the above claims, characterized in that the component is attached to the metal layer (5) beneath it with the aid of a conductive adhesive.

11. A method according to any of the above claims, characterized in that the top surface of the component (8) is a light emitting or receiving component.

12. A circuit board, which comprises

- an optical component (8), and
- an optical bus (3), through which an optical signal can be led to the component or away from the component,

characterized in that the component (8) is at least partly embedded inside the circuit board, in such a way that the component comes into optical contact with the optical bus and that the component (8), which comprises on one side both an optically active area (11) and at least one conductive area (10, 12), is set in place in such a way that the optically active area (11) of the component is at essentially right angles to the plane of the circuit board.

13. A circuit board according to claim 12, characterized in that the component (8) is embedded inside the circuit board, in such a way that the component is located entirely between the first and second surface of the circuit board.

14. A circuit board according to claim 12 or 13, characterized in that the space between the optically active area (11) of the component (8) and the optical bus (3) is filled with the same material as the optical bus (3).

15. A circuit board according to claim 14, characterized in that the component (8) comprises a first conductor material area (12) and a second conductor material area (10), and from which first conductor material area (12) an electrical contact is formed with the circuit board's first conductor layer (1) and from which second conductor material area (10) an electrical contact is formed with the circuit board's second conductor layer (1) that is at a different level in the thickness direction of the circuit board.

16. A circuit board according to any of the above claims, characterized in that the top surface of the component is a light emitting or receiving component.